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## RESEARCH INTERESTS

- **Runtime Reconfiguration** (architectures, idle function elimination, self-reconfiguration)
- **High-performance systems** (big-data systems, heterogeneous clusters, communication network)
- **Design automation** (high-level analysis, high-level synthesis, reconfiguration-driven compiler)

## EDUCATION

- **Imperial College London**, London, UK, Oct. 2011 - May. 2015
  PhD in Computing, supervised by Prof. Wayne Luk
  Thesis Topic: "Optimising Runtime Reconfigurable Designs for High Performance Applications"
- **Imperial College London**, London, UK, Oct. 2010 - Sep. 2011
  MSc in Analogue and Digital IC Design, supervised by Prof. Wayne Luk (Grade: Distinction)
  Thesis Topic: "Combining Wireless Network with Heterogeneous Cluster"
- **Fudan University**, Shanghai, China, Sep. 2006 - Aug. 2010
  BS in Electronic Engineering, supervised by Prof. Hao Min (Grade: 3.70/4.00)
  Thesis Topic: "Research on Digital Automatic Gain Control (DAGC) and Analogue Front-End for Radio Frequency Identification (RFID) System"

## AWARDS

- **Awards**
  - EPSRC Pathway to Impacts Award, 2014
  - Santander Mobility Award, 2014
  - Award for Outstanding Achievement in the MSc in Analogue and Digital Integrated Circuit Design, Imperial College London, 2011
  - Outstanding Graduate Award, Shanghai, 2010
  - Excellent student Award, Fudan University, 2008
- **Scholarship**
  - Nation Scholarship, Fudan University, 2009
  - People Scholarship, Fudan University, 2008
  - University Scholarship, Fudan University, 2007

## RESEARCH EXPERIENCE

- **Maximising Impact of Novel Reconfigurable Architecture (Pathways to Impact)** *Sep. 2014 - Jun. 2015*
  - *Objective*: developing prototypes for EURECA architectures
  - *Achievements*:
    - EURECA chip developed in 130-nm SMIC technology (to be fabricated at Sep. 2015)
    - Initial EURECA compiler
- **Custom Computing for Advanced Digital Systems (EP/I012036/1)** *Nov. 2010 - present*
  - *Objective*: exploring reconfigurable systems for high-performance applications
  - *Achievements*:
    - EURECA: a novel architecture that supports complex data access operations [$C16$]

    - Climate modelling applications with inexact computation [$C17$]
    - Session types for scalable reconfigurable systems [$C3$], [$J1$]
    - Adaptive heterogeneous clusters with wireless monitoring network [$C1$], [$C2$]

- **Self Improving Compression Accelerator (SICA)** *Feb. 2015 - present*
    - *Objective*: runtime reconfigurable compression engines to improve compression performance
    - *Achievements*:
        - SICA: compression tool that adapts algorithm parameters based on monitored results

- **FASTER Project (grant number 248976)** *Oct. 2011 - Dec. 2014*
    - *Objective*: developing tools and approaches for runtime reconfiguration
    - *Achievements*:
        - Approach to reconfigure idle functions into active functions [$C7$], [$C8$], [$C9$], [$C10$], [$J4$], [$J5$]
        - EXPRESS: open-source tool to automate the idle-function elimination technique [$C6$], [$C10$], [$C11$]

- **EPICS Project (grant number 257906)** *Jan. 2013 - Dec. 2013*
    - *Objective*: adaptive designs based on runtime reconfiguration
    - *Achievements*:
        - Self-tuned arithmetic operators for finite-difference algorithms [$C5$], [$J2$]
        - Power-adaptive approach for Energy Harvesting Systems [$J3$]

## WORK AND VISITING EXPERIENCE

- **Department of Computing, Imperial College London**, London, UK
    - *Research Associate* **May. 2015 - present**
      Major tasks: academic research, project management, student supervision, teaching assistance and system administration.
    - *Research Assistant* **Oct. 2011 - May. 2015**
      Major tasks: academic research, project management, teaching assistance and system administration.

- **School of Microelectronics, Fudan University**, Shanghai, China
    - *Visiting Scholar* **May. 2015 - Jul. 2015**
      Major tasks: leading a collaboration to build EURECA chip prototype.

- **Department of Electronic Information, Politecnico di Milano**, Milan, Italy
    - *Visiting Scholar* **Sep. 2014 - Oct. 2014**
      Major tasks: leading a collaboration to apply EXPRESS tool to image processing applications.

## PATENT

**X. Niu** and W. Luk, "Reconfigurable Integrated Circuit with On-Chip Configuration Generation", Patent application number: 1414286.3. PCT application number PCT/GB2015/052331

## PUBLICATIONS

### Peer-reviewed Journal Publications

[$J6$] P. D. Düben, F. P. Russell, **X. Niu**, W. Luk, T. N. Palmer. "On the Use of Programmable Hardware And Reduced Numerical Precision In Earth System Modelling". Journal Of Advances in Modelling Earth Systems (JAMES), accepted manuscript online: 20 August 2015

[$J5$] T.C.P. Chau, **X. Niu**, A. Eele, W. Luk, P.Y.K. Cheung and J. Maciejowski. "Extended Heterogeneous Reconfigurable System for Adaptive Particle Filters with Data Compression". ACM Transactions on Reconfigurable Technology and Systems (TRETS) 7(4): 36:1-36:17, 2015.

[$J4$] **X. Niu**, Q. Jin, W. Luk, Q. Liu and O. Pell. "Automating Elimination of Idle Functions by Run-time Reconfiguration". ACM Transactions on Reconfigurable Technology and Systems (TRETS) 8(3): 15, 2015.

[$J3$] Q. Liu, T. Mak, T. Zhang **X. Niu**, W. Luk and A. Yakovlev. "Power Adaptive Computing System Design

for Solar Energy Powered Embedded Systems". IEEE Transactions on Very Large Scale Integration Systems (TVLSI) 23(8): 1402-1414, 2015.

[$J2$] **X. Niu**, Q. Jin, W. Luk and S. Weston. "A Self-Aware Tuning and Evaluation Method for Finite-Difference Applications in Reconfigurable Systems". ACM Transactions on Reconfigurable Technology and Systems (TRETS) 7(2): 15:1-15:19, 2014.

[$J1$] N. Ng, N. Yoshida, **X. Niu** and K.H. Tsoi. "Session Types: Towards Safe and Fast Reconfigurable Design". SIGARCH Computer Architecture News 40(5), 22-27, 2012.

**Peer-reviewed Conference Publications**

[$C19$] J. S. Targett, **X. Niu**, F. P. Russell, W. Luk, S. Jeffress, P. D. Düben ,T. N. Palmer."Lower Precision for Higher Accuracy: Precision and Resolution Exploration for Shallow Water Equations", International Conference on Field Programmable Technology (FPT), 2015 (accepted).

[$C18$] J. Xie, **X. Niu**, A. K.S. Lau, K. K. Tsia and H. K.H. So. "Accelerated Cell Imaging and Classification on FPGAs for Quantitative-phase Asymmetric-detection Time-stretch Optical Microscopy", International Conference on Field Programmable Technology (FPT), 2015 (accepted).

[$C17$] F. P. Russell, P. D. Düben, **X. Niu**, W. Luk, T. N. Palmer. "Architectures and precision analysis for modelling atmospheric variables with chaotic behaviour", IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM), pp. 171-178, 2015.

[$C16$] **X Niu**, W. Luk, Y. Wang. "EURECA: On-Chip Configuration Generation for Effective Dynamic Data Access", ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA), pp.74- 83, 2015.

[$C15$] A. Bara, **X. Niu**, W. Luk. "A Dataflow System for Anomaly Detection and Analysis", International Conference on Field Programmable Technology (FPT), pp. 276-279, 2014.

[$C14$] P. Grigoras, M. Tottenham, **X. Niu**, J. G.F. Coutinho and W. Luk. "Elastic Management of Reconfigurable Accelerators", IEEE International Symposium on Parallel and Distributed Processing with Applications (ISPA), pp. 174-181, 2014.

[$C13$] **X. Niu**, J.G.F. Coutinho, W. Yu and W. Luk. "Dynamic Stencil: Effective Exploitation of Run-time Resources in Reconfigurable Clusters". International Conference on Field Programmable Technology (FPT), pp. 214-221, 2013.

[$C12$] **X. Niu**, J.G.F. Coutinho and W. Luk. "A Scalable Design Approach for Stencil Computation on Reconfigurable Clusters", International Conference on Field-programmable Logic and Applications (FPL). pp. 1-4, 2013.

[$C11$] R. Cattaneo, **X. Niu**, C. Pilato, T. Becker, M.D. Santambrogio and W. Luk. "A Framework for Effective Exploitation of Partial Reconfiguration in Dataflow Computing". International Symposium on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC) pp. 1-8, 2013.

[$C10$] P. Grigoras, **X. Niu**, J.G.F. Coutinho and W. Luk. "Aspect Driven Compilation for Dataflow Designs". IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP), pp 18-25, 2013.

[$C9$] **X. Niu**, T.C.P. Chau, Q. Jin, W. Luk and Q. Liu. "Automating Elimination of Idle Functions by Runtime Reconfiguration". IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM), pp. 97-104, 2013.

[$C8$] T.C.P. Chau, **X. Niu**, Alison Eele, W. Luk, Peter Y.K. Cheung and Jan Maciejowski. "Heterogeneous Reconfigurable System for Adaptive Particle Filters in Real-Time Applications". International Symposium on Applied Reconfigurable Computing (ARC), pp. 1-12, 2013.

[$C7$] **X. Niu**, T.C.P. Chau, Q. Jin, W. Luk and Q. Liu. "Automating Resource Optimisation in Reconfigurable Design". ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA), pp 275, 2013.

[$C6$] K. Papadimitriou, C. Pilato, D.N. Pnevmatikatos, M.D. Santambrogio, C.B. Ciobanu, T. Todman, T. Becker, T. Davidson, **X. Niu**, G. Gaydadjiev, W. Luk, D. Stroobandt. "Novel Design Methods and a Tool Flow for Unleashing Dynamic Reconfiguration". IEEE International Conference on Computational Science and Engineering (CSE), pp. 391-398, 2012.

[$C5$] **X. Niu** and W. Luk. "A Dynamically Tuned Finite Difference Method For Reconfigurable Systems". 2012 Workshop on Self-Awareness in Reconfigurable Computing Systems (SRCS).

[$C4$] **X. Niu**, Q. Jin, W. Luk and Q. Liu. "Exploiting Run-time Reconfiguration in Stencil Computation". International Conference on Field-programmable Logic and Applications (FPL), pp. 173-180, 2012.

[$C3$] N. Ng, N. Yoshida, **X. Niu**, K.H. Tsoi, and W. Luk. "Session Types: Towards Safe and Fast Reconfigurable Design". International Symposium on Highly Efficient Accelerators and Reconfigurable Technologies (HEART), pp. 22-27, 2012.

[$C2$] **X. Niu**, K.H. Tsoi and W. Luk. "Self-Adaptive Heterogeneous Cluster with Wireless Network". Reconfigurable Architectures Workshop (RAW), pp. 306-311, 2012.

[$C1$] **X. Niu**, K.H. Tsoi, W. Luk. "Reconfiguring Distributed Applications in FPGA Accelerated Cluster with Wireless Networking". International Conference on Field-programmable Logic and Applications (FPL), pp. 545-550, 2011.

**Book Chapter**

[$B1$] **X. Niu**, T. Todman, and W. Luk. "Self-Adaptive Hardware Acceleration on a Heterogeneous Cluster". Self-aware Computing Systems: an Engineering Approach, Chapter 9. Springer, 2015.

## INVITED SEMINARS AND PRESENTATIONS [$^{\star} Presenters$]

4. **X. Niu**$^{\star}$ "EURECA: On-Chip Configuration Generation for Effective Dynamic Data Access". Microelectronic Building, Fudan University, invited by Prof. Lingli Wang, 2015.

3. **X. Niu**$^{\star}$ "Run-time Reconfigurable Design: Analysis and Optimisation". Summer School on Accelerating Scientific Computing, Huxley Building, Imperial College London, invited by Prof. Wayne Luk, 2013.

2. **X. Niu**$^{\star}$ "Self-Adaptive Heterogeneous Computing with Wireless Network". Electronic Engineering Building, Tianjin University, invited by Prof. Qiang Liu, 2012

1. **X. Niu**$^{\star}$ "Axel: Self-Adaptive Heterogeneous Computing". Luo Mu Building, Tsinghua University, invited by Prof. Yu Wang. 2012.

## CONTRIBUTED CONFERENCE AND WORKSHOP PRESENTATIONS [$^{\star} Presenters$]

17 F. P. Russell$^{\star}$, P. D. Düben, **X. Niu**, W. Luk, T. N. Palmer. "Architectures and precision analysis for modelling atmospheric variables with chaotic behaviour", FCCM, Vancouver, Canada, 05/2015.

16 **X Niu**, W. Luk, Y. Wang. "EURECA: On-Chip Configuration Generation for Effective Dynamic Data Access", FPGA, Monterey, USA, 02/2015.

15 A. Bara, **X. Niu**$^{\star}$, W. Luk. "A Dataflow System for Anomaly Detection and Analysis", International Conference on Field Programmable Technology (FPT), Shanghai, China, 12/2014.

14 P. Grigoras$^{\star}$, M. Tottenham, **X. Niu**, J. G.F. Coutinho and W. Luk. "Elastic Management of Reconfigurable Accelerators", IEEE International Symposium on Parallel and Distributed Processing with Applications (ISPA). Milan, Italy, 08/2014.

13 **X. Niu**$^{\star}$, J.G.F. Coutinho, W. Yu and W. Luk. "Dynamic Stencil: Effective Exploitation of Run-time Resources in Reconfigurable Clusters". International Conference on Field Programmable Technology (FPT). Kyoto, Japan, 2013.

12 **X. Niu**$^{\star}$, J.G.F. Coutinho and W. Luk. "A Scalable Design Approach for Stencil Computation on Reconfigurable Clusters", International Conference on Field-programmable Logic and Applications (FPL). Porto, Portugal, 09/2013.

11 R. Cattaneo$^{\star}$, **X. Niu**, C. Pilato, T. Becker, M.D. Santambrogio and W. Luk. "A Framework for Effective Exploitation of Partial Reconfiguration in Dataflow Computing". International Symposium on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC) . Darmstadt, Germany, 07/2013.

10 P. Grigoras, **X. Niu**, J.G.F. Coutinho and W. Luk$^{\star}$. "Aspect Driven Compilation for Dataflow Designs". IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP). Washington, USA, 06/2013.

9 **X. Niu**⋆, T.C.P. Chau, Q. Jin, W. Luk and Q. Liu. "Automating Elimination of Idle Functions by Run-time Reconfiguration". FCCM. Seattle, USA, 04/2013.

8 T.C.P. Chau⋆, **X. Niu**, Alison Eele, W. Luk, Peter Y.K. Cheung and Jan Maciejowski. "Heterogeneous Reconfigurable System for Adaptive Particle Filters in Real-Time Applications". International Symposium on Applied Reconfigurable Computing (ARC). Los Angeles, USA, 03/2013.

7 **X. Niu**, T.C.P⋆. Chau, Q. Jin, W. Luk and Q. Liu. "Automating Resource Optimisation in Reconfigurable Design". FPGA. Monterey, USA, 02/2013.

6 K. Papadimitriou⋆, C. Pilato, D.N. Pnevmatikatos, M.D. Santambrogio, C.B. Ciobanu, T. Todman, T. Becker, T. Davidson, **X. Niu**, G. Gaydadjiev, W. Luk, D. Stroobandt. "Novel Design Methods and a Tool Flow for Unleashing Dynamic Reconfiguration". IEEE International Conference on Computational Science and Engineering (CSE). Paphos, Cyprus, 12/2012.

5 **X. Niu**⋆ and W. Luk. "A Dynamically Tuned Finite Difference Method For Reconfigurable Systems". Workshop on Self-Awareness in Reconfigurable Computing Systems (SRCS). Oslo, Norway, 09/2012.

4 **X. Niu**⋆, Q. Jin, W. Luk and Q. Liu. "Exploiting Run-time Reconfiguration in Stencil Computation". International Conference on Field-programmable Logic and Applications (FPL). Oslo, Norway, 09/2012.

3 N. Ng, N. Yoshida, **X. Niu**, K.H. Tsoi, and W. Luk⋆. "Session Types: Towards Safe and Fast Reconfigurable Design". International Symposium on Highly Efficient Accelerators and Reconfigurable Technologies (HEART). Okinawa, Japan, 05/2012.

2 **X. Niu**⋆, K.H. Tsoi and W. Luk. "Self-Adaptive Heterogeneous Cluster with Wireless Network". Reconfigurable Architectures Workshop (RAW). Shanghai, China, 05/2012.

1 **X. Niu**⋆, K.H. Tsoi, W. Luk. "Reconfiguring Distributed Applications in FPGA Accelerated Cluster with Wireless Networking". International Conference on Field-programmable Logic and Applications (FPL). Chania, Greece, 09/2011.

## TEACHING

- **Course Support Leader** 2014 - present
  *Second-Year Computer Architecture* Help preparing lecture notes, organising tutorials, collecting student feedbacks, answering student questions, and marking student answer sheets.
- **Course Support Leader** 2012 - 2014
  *First-Year Computer Architecture* Help preparing lecture notes, organising tutorials, answering student questions, and marking student answer sheets.

## RESEARCH MENTORING

- **Summer Students** 2014 - present
  *Bisheng Huang* Accelerating Lz77 Algorithm On Reconfigurable Systems.
  Accelerating Lz77 modules, exploiting hashing functions that minimise conflicts

  *Shengtao Xu* Accelerating Arithmetic and Huffman Algorithms On Reconfigurable Systems.
  Accelerating coding modules, evaluation of coding techniques

  *Junyi Xie* Optimising classification techniques for medical images.
  Accelerating classification system with Quantitative Phase Imaging (QPI) and Support Vector Macine (SVM)
  Paper published at FPT'2015 [$C18$]

- **MRes Student 2014- present**
  *James Stanley Targett* Exploiting Accuracy Trade-offs in High-Performance Applications.
  Accelerated Shallow-Water Equations, precision optimisation techniques that enable accelerated applications to achieve higher climate modelling accuracy with lower computational precision
  Paper published at FPT'2015 [$C19$]

- **MEng Student 2013 - present**
  *Andrei Bara* DeADA: A Dataflow Engine for Anomaly Detection and Analysis
  Developing and accelerating novel techniques to detect network intrusion
  Paper published at FPT'2014[$C15$]

**Distinguished Project Award**

*Paul Grigoras* Aspect Driven Compilation for Dataflow Designs
Compiler to automatically apply coarse-grained runtime reconfiguration techniques
Paper published at ASAP'2013[*C*10]
**Finalist for Science and Technology Awards, UK**
**ARM Project Prize**

## PROFESSIONAL SERVICE

- **Peer Reviewer**
  FPT, FPL, FPGA, FCCM, HEART, ReConFig, IEEE TCAD, ACM TRETS
- **Conference and Summer School Organisation**
  Organising committee, FPL 2015
  Help organising the second OpenSPL Symposium and Summer School, 2015
  Help organising the first OpenSPL Symposium and Summer School, 2014
  Help organising Imperial College Summer School on Accelerating Scientific Computation, 2013